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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,557	07/22/2003	Takashi Ipposhi	240586US2	5909

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,557	IPPOSHI, TAKASHI	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-13,15,16 and 18* is/are rejected.

7)☒ Claim(s) *14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants amendment filed June 29, 2004.

Specification

The objection to the title of the invention as being not descriptive has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,111,280) in view of Ipposhi et al. (US 2003/0094674 A1).

Gardner et al. teach a 1. A semiconductor device comprising: an SOI substrate including a supporting substrate 2, an oxide film layer 3 and an SOI (Semiconductor-On-Insulator) layer 4 which are sequentially deposited; and a MIS (Metal Insulator Semiconductor) transistor 6 including a gate insulating film 10 formed on the SOI layer, a gate electrode 11 formed on the gate insulating film and a source/drain active layer 7 & 8 formed in the SOI layer so as to be adjacent to a portion under the gate electrode, wherein at least a portion of the supporting

substrate which is located under the MIS transistor is removed, to form a hollow portion (Figure 3, cols 3 and 5, lines 13-67 and 1-21, respectively).

However, Gardner et al. fail to teach the supporting substrate and the SOI layer having crystal directions different from each other.

Ipposhi et al. teach a supporting substrate 1 and the SOI layer 3 having crystal directions different from each other (Figure 2, page 4, paragraph [0060]).

In regard to claims 15 and 18, Ipposhi et al. teach a <110> crystal direction of the supporting substrate corresponds to a <100> crystal direction of the SOI layer (Figure 2, page 4, paragraph [0060]).

Since Gardner et al. and Ipposhi et al. are from the same field of endeavor (SOI semiconductor devices), the purpose disclosed by Ipposhi et al. would have been recognized in the pertinent art of Gardner et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made modify the SOI semiconductor device structure as taught by Gardner et al. with the SOI semiconductor device structure having a supporting substrate and the SOI layer having crystal directions different from each other as taught by Ipposhi et al. to develop a semiconductor wafer (abstract).

Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamic, Jr. (6,084,284) in view of Ipposhi et al. (US 2003/0094674 A1).

Adamic, Jr. teaches a semiconductor device comprising: an SOI substrate including an oxide film layer 270 serving as a bottom of the semiconductor device and an SOI (Semiconductor-on-Insulator) layer which are sequentially deposited; a MIS (Metal Insulator

Semiconductor) transistor including a gate insulating film 812 formed on the SOI layer, a gate electrode 811 formed on the gate insulating film and a source/drain active layer 822 & 833 formed in the SOI layer so as to be adjacent to a portion under the gate electrode; an interlayer insulating film 215 covering the MIS transistor; and a supporting substrate 224 bonded 219, 221 & 226 to the interlayer insulating film (Figures 1-2F and 8; col. 4, lines 14-20; cols. 9-10, lines 39-67 and 1-44, respectively; col. 16, lines 9-16). In regard to claim 7 Adamic, Jr. teaches a metal film 256 covering a surface of the oxide film layer (Figure 2F).

However, Adamic, Jr. fail to teach the supporting substrate and the SOI layer having crystal directions different from each other.

Ipposhi et al. teach a supporting substrate 1 and the SOI layer 3 having crystal directions different from each other (Figure 2, page 4, paragraph [0060]).

Since Adamic, Jr. and Ipposhi et al. are from the same field of endeavor (SOI semiconductor devices), the purpose disclosed by Ipposhi et al. would have been recognized in the pertinent art of Adamic, Jr. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made modify the SOI semiconductor device structure as taught by Adamic, Jr. with the SOI semiconductor device structure having a supporting substrate and the SOI layer having crystal directions different from each other as taught by Ipposhi et al. to develop a semiconductor wafer (abstract).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,111,280) and Ipposhi et al. (US 2003/0094674 A1) as applied to claims 10, 15 and 18 above, and further in view of Murata et al. (US 6,601,452 B2).

Gardener et al. and Ipposhi et al. teach all mentioned in the rejection above. However, Gardner et al. and Ipposhi et al. fail to teach the hollow portion surrounded by four end faces of the supporting substrate, each of the four end faces being exposed in the hollow portion and being a (111) plane. Murata et al. teach the hollow portion surrounded by four end faces of the supporting substrate, each of the four end faces being exposed in the hollow portion and being a (111) plane (Figure 13-14C, col. 7-8, lines 55-67 and 1-2, respectively). Since Gardner et al., Ipposhi et al. and Murata et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Murata et al. would have been pertinent in the art of Gardner et al. and Ipposhi et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device as taught by Gardner et al. and the SOI semiconductor device structure having a supporting substrate and the SOI layer having crystal directions different from each other as taught by Ipposhi et al. with the substrate as taught by Murata et al. to improve the bonding strength (col. 7, lines 47-51).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,111,280) and Ipposhi et al. (US 2003/0094674 A1) as applied to claims 10, 15 and 18 above, and further in view of Sakai et al. (US 6,229,165 B1).

Gardener et al. and Ipposhi et al. teach all mentioned in the rejection above. Gardner et al. further teach a portion of the oxide film layer 3 exposed in the hollow portion (Figure 2). However, Gardner et al. and Ipposhi et al. fail to teach a metal film 141 covering a surface of the supporting substrate 121 including an end face (left substrate side) in the hollow portion (Figures 9-10, cols. 6-7, lines 9-14 and 53-67, respectively). Since Gardner et al., Ipposhi et al. and Sakai

et al. are from the same field of endeavor (semiconductor devices having substrates with hollow portions), the purpose disclosed by Sakai et al. would have been pertinent in the art of Gardner et al. and Ipposhi et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device as taught by Gardner et al. and the SOI semiconductor device structure having a supporting substrate and the SOI layer having crystal directions different from each other as taught by Ipposhi et al. with the metal film as taught by Sakai et al. to enhance light transmission prevention capability (col. 7, lines 67-66).

Allowable Subject Matter

Claims 14 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to SOI semiconductor devices:

Umezawa et al. (US 2003/0128809 A1) Yamada et al. (US 2003/0057487 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
August 30, 2004

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